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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/593,695	NAKASHIMA, YASUHIKO	
	Examiner	Art Unit	
	IDRISS N. ALROBAYE	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *18-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/20/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This action is responsive to supplemental response received on 6/18/2010.

2. Claims 1-17 are presented for examination.

3. Claims 18-29 are withdrawn.

4. Claims 30-31 are cancelled.

Continued Examination Under 37 CFR 1.114

5. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/18/2010 has been entered.

Specification

6. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract is not clearly written, the abstract language should be clear and concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains.

For instance, it's not clear what applicant meant by "A rows AND comparison section MR performs a logical AND of row elements..." Therefore, it's suggested to re-write the abstract in a clear and concise way to represent the technical disclosure of the invention.

Claim Objections

7. Claim 5 is objected to because of the following informalities: As per claim 5, the claim recites "wherein a readout from the register and/or the main...", it should be changed to --wherein a readout operation from the register and/or the main...-- Also, throughout the claim, the term 'readout' should be followed with 'operation' to increase clarity. Appropriate correction/clarification is required.

8. Claim 6 is objected to because of the following informalities: As per claim 6, the claim recites "*includes a rows "AND" operation comparison",* it should be changed to – includes a row of "AND" operation comparison". Appropriate correction is required.

9. Claim 7 has similar issues as in claim 6 with respect to "a rows AND comparison". Also, claim 7 last line recites "*...other row elements are all a logical "0".",* it should be changed to --...other row elements are all logical "0". Appropriate correction is required.

10. Claim 14 is objected to because of the following informalities: As per claim 5, the claim recites "where a readout from the register and/or the main...", it should be changed to --where a readout operation from the register and/or the main...-- Also, throughout the claims, the term 'readout' should be followed with 'operation' to increase clarity. Appropriate correction/clarification is required.

Claim Rejections - 35 USC § 112

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

13. As per claim 1, the claim recites "input/output group generating programmed logic circuitry configured to generate an input/output (I/O) group..." The underlined limitation is vague and unclear. It's not clear from the claim language what's meant by I/O group generating programmed logic circuitry. It's also not clear how the programmed logic circuitry generates an I/O group. As well known in the art, an I/O is understood to be a hardware input as in an input port which takes data and hardware output as in an output which outputs data. However, it is not clear how hardware input port or output port generates 'programmed logic circuitry'. It's is also not clear how the 'programmed logic circuitry' generates 'I/O group'. Appropriate correction/clarification is required.

Claim 1, page 3 recites "*wherein said instruction region storage section further includes an I/O group storage portion used to store the I/O group…"* it's not clear how the instruction region storage stores 'the I/O group'. From the claim language, it appears that the I/O group are hardware component, so it's not clear how a hardware 'I/O group' is stored in the instruction region. Furthermore, the claim uses past tense as in 'used', it is suggested to use present since it implies from the current claim language that the 'instruction region storage' used to store but not anymore. Appropriate correction/clarification is required.

Claim 1, page 3 recites "*upon matching an input pattern in the instruction region with an input pattern in the input/output group..."* this limitation is vague and indefinite. The previous limitation shows that the I/O group is part of the instruction region storage, however now the pattern of the I/O group (which is part of the instruction region) is compared with the pattern of 'the instruction region'. It appears that the pattern is compared against itself. Appropriate correction/clarification is required.

Claim 1, page 3 further recites "*input/output group setting programmed logic circuitry configured, based on stored dependency relations information, to set an input/output group…"* this limitation is vague and indefinite. It's not clear whether the 'input/output group setting programmed logic circuitry is a name 'label' or a function to set the programmed logic circuitry. It's also not clear whether the term 'configured' is referred back to the I/O group or to the programmed logic circuitry. It implies that the term 'configured' refers back to the I/O group but it also configures...to set itself as

indicated in the underlined limitation above 'to set an input/output group'. Appropriate correction/clarification is required.

14. Claim 2, page 4 recites the limitation "the input/output group programmed logic circuitry". There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

15. Claim 5, page 5 recites "in the dependency relations storage section..." in various limitations of the claim, there is insufficient antecedent basis for this limitation in the claim. It should be changed to --in the dependency relations storage memory section...-- Appropriate correction is required.

Claim 5, page 5 recites "*temporarily storing a provisional matrix comprising a row element of the dependency relations storage section, wherein said row element corresponds to the output element",* this limitation is vague and unclear. It appears that the matrix is a hardware component since it comprises a row of the dependency relations storage section, however it's not clear how it's a hardware matrix is temporarily stored. Note the hardware matrix is also mentioned in other limitation of the claim, the rejection above applies to it as well. Appropriate correction/clarification is required.

16. As per claim 8, the claim recites "*by the first computing means, the second computing means subject*...", the underlined limitations fail to provide sufficient antecedent basis in the claim. Appropriate correction is required.

17. As per claim 9, the claim recites in the last two limitations "...while the input/output group is generated..." this limitation is vague and indefinite. It's not clear how the I/O group is generated. As explained above, it implies from the claim that the I/O are hardware ports, therefore it is not clear how a hardware I/O is generated. Furthermore, claim 9 recites "*a temporal storage section which stores a changed dependency relations between...*" it's not clear how a changed dependency relations is stored, perhaps applicant meant 'storing information of a changed dependency relations'. Appropriate correction/clarification is required.

18. As per claim 10, the claim has similar issue as in claim 9 with respect to "...while the input/output group is generated...'. Appropriate correction is required. Furthermore, the claim recites "...allocated to the output element and/or the input element", the input and output elements lack of antecedent basis in the claim. Appropriate correction/clarification is required.

19. Claim 5 is objected to because of the following informalities: As per claim 5, the claim recites "wherein a readout from the register and/or the main...", it should be changed to --wherein a readout operation from the register and/or the main...-- Also, throughout the claim, the term 'readout' should be followed with 'operation' to increase clarity. Appropriate correction/clarification is required.

20. As per claim 13, the claim has similar issue as in claim 9 with respect to "...while the input/output group is generated..." Appropriate correction is required.

21. Note the claim language as currently recited is in coherent and replete with grammatical errors. The claim language is thus indefinite and is interpreted by the examiner as broadly as reasonably possible. It is suggested that the applicant's re-write the claims in order to receive a proper and more accurate prosecution.

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 1-4, 8-11, 13, 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miki U.S. Patent No. 6,810,474 in view of Huang U.S. Patent No. 4,943,909.

24. As per claim 1, Miki teaches a data processing device which reads out program instructions from an instruction region in a main memory and writes a result of a computation into the main memory (see Fig. 1 and col. 4, lines 8-41),

the data processing device comprising:

first stream processor including programmed logic circuitry configured to perform computations based on one or more instructions in the instruction region which are read out from the main memory (see Fig. 1, and col. 4, lines 35-40);

a register by which the first stream processor writes data and reads to/from the main memory (Fig. 1, element 118);

input/output group generating programmed logic circuitry configured to generate an input/output (I/O) group at a time of execution of one or more program instructions in the instruction region, said I/O group having an input pattern comprising one or more input elements and an associated output pattern comprising one or more output elements (Fig. 3, and col. 8, lines 43-67); and

a memory, distinct from said main memory, having an instruction region storage section dedicated for storing data used for reusing certain instructions, wherein said instruction region storage section further includes an I/O group storage portion used to store the I/O group (Fig. 3 and col. 8, line 43 to col. 9, line 8; see also col. 9, line 62 to col. 10, line 26; note the cache in Fig. 1 is the claimed memory), and wherein

at the time of execution of one or more instructions read out from the instruction region in the main memory, upon matching an input pattern in the instruction region input pattern in the input/output group, the first stream processor performs a reuse operation that outputs the associated output pattern to the register and/or the main memory (Fig. 3 and col. 8, line 43 to col. 9, line 8; see also col. 9, line 62 to col. 10, line 26), and further wherein

the input/output group generating programmed logic circuitry includes a dependency relations storage memory section and also generates dependency relations information, which is stored in the dependency relations storage memory section, that identifies input values and input addresses, for a register/memory from which a readout operation is performed, corresponding to input elements in the input pattern of the input/output group from which each output value and output address, for a register/memory to which a writing operation is performed, corresponding to output elements in an associated output pattern is derived.

Miki shows dependency relations storage (see col. 2, line 8-44) but did not specifically go into the details of input element and output element derives. However, Huang teaches identifies input values and input addresses, for a register/memory from which a readout operation is performed, corresponding to input elements in the input pattern of the input/output group from which each output value and output address, for a register/memory to which a writing operation is performed, corresponding to output elements in an associated output pattern is derived; and input/output group setting programmed logic circuitry configured, based on stored dependency relations information, to set an input/output group that is made up of an output pattern including at least one said output element and an input pattern including at least one said input element (see Huang, Fig. 3 and col. 5, lines 16-51), for the purpose of realization of any computing function with a regular array of interconnected processing elements.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Huang in invention of Miki,

for the purpose of realization of any function within a regular array of interconnected elements thus allowing highly parallel computations which significantly improves performances.

25. As per claim 2, Miki in view of Huang further teaches the data processing device as defined in claim 1, wherein,

if a first group of input elements from which a first output element is derived, is included entirely within a second group of input elements from which a second output element different from the first output element is derived, the input/output group programmed logic circuitry sets (i) the second group as the input pattern and (ii) the first group and the second group as the output pattern (see Huang, col. 5, lines 16-67 and see also Miki col. 8, lines 43-67).

26. As per claim 3, Miki in view of Huang further teaches the data processing device as defined in claim 1, wherein,

If there is no shared input element between a first group of input elements from which a first output element is derived, and a second group of input elements from which a second output element different from the first output element is derived, the input/output pattern group setting programmed logic circuitry sets (i) a first input/output group in which the first group of the input elements is the input pattern and the first output element is the output pattern and (ii) a second input/output group in which the second group of the input elements is the input pattern and the second output element

is the output pattern (see Huang, col. 5, lines 16-67 and see also Miki col. 8, lines 43-67).

27. As per claim 4, Huang further teaches the data processing device as defined in claim 1, wherein

the dependency relations storage section is made up of a two-dimensional (2D) matrix-arranged memory portion in which row elements of the matrix-arranged memory are stored with the output elements and column elements of the matrixed-arranged memory are stored with the input elements, and each memory of the 2D matrix-arranged memory includes information indicating whether or not an output element corresponding to a row element is derived from an input element corresponding to a column element (see Huang, Fig. 3 and col. 5, lines 16-67).

28. As per claim 8, Huang further teaches the data processing device as defined in any claim 1, further comprising at least one second stream processor including programmed logic circuitry configured to perform computations on instructions int eh instruction region,

wherein with respect to instructions in the instruction region processed by the first computing means, the second computing means subjects instructions in the instruction region to a computation based on a predicted input value, and registered a result of the computation in the instruction region storage means (col. 5, lines 16-51).

29. As per claim 9, Miki further teaches the data processing device as defined in claim 1, wherein,

the input/output group setting programmed logic circuitry further comprises: an output-side group storage section which stores information of an input/output group to which each of the output elements belongs; an input-side group storage section which stores information of an input/output group to which each of the input elements belongs; a temporal storage section which stores a changed dependency relation between an output element and an input element, whenever there is a change in information stored in the dependency relations storage section while the input/output group is generated; and a group temporal storage section which stores information of a changed input/output group when there is a change in information stored in the dependency relations storage section while the input/output group is generated (Fig. 3, and col. 8, lines 43-67 and col. 4, lines 35-40).

30. As per claim 10, Miki further teaches the data processing device as defined in claim 9, wherein

the input/output group setting programmed logic circuitry further includes a group management section that stores information of the input/output group which has previously been allocated to the output element and/or the input element while the input/output group is generated (Fig. 3, and col. 8, lines 43-67 and col. 8, line 43 to col. 9, line 8),

31. As per claim 11, Huang further teaches the data processing device as defined in claim 9, wherein

the dependency relations storage section is made up of a two-dimensional (2D) matrix-arranged memory portion in which row elements of the matrix-arranged memory are stored with the output elements and column elements of the matrix-arranged memory are stored with the input elements, and each memory element of the 2D matrix-arranged memory includes information indicating whether or not an output element corresponding to a row element is derived from an input element corresponding to a column element (see Huang, Fig. 3 and col. 5, lines 16-67).

32. As per claim 13, Miki further teaches the data processing device as defined in claim 9, wherein

the input/output group setting programmed logic circuitry further includes a conditional branch storage section that stores information regarding an input element on which the conditional branch instruction depends whenever a conditional branch instruction is detected while the input/output group is generated (see col. 4, lines 8-41).

33. As per claim 15, Miki further teaches the data processing device as defined in claim 1, wherein, the instruction region storage section includes input pattern storage section which stores input patterns as a tree structure in which items that are to be subjected to equal comparison are regarded as nodes (Fig. 3, and col. 8, lines 43-67).

34. As per claim 16, Miki further teaches the data processing device as defined in claim 15,

further comprising input pattern storage means that organizes the tree structure in such a manner that a value of an item in the input pattern, which item is subjected to equal comparison, is stored in association with an item which is to be next subjected to a comparison (see col. 8, lines 15-67).

35. As per claim 17, Huang further teaches the data processing device as defined in claim 16, wherein, the input pattern storage programmed logic circuitry further includes associative search performing programmed logic circuitry and an additional information storage section, wherein the associative search performing programmed logic circuitry utilizes one or more search target lines that include a value storage portion in which a value of an item to be subjected to equal comparison is placed, and a key storage portion in which a key for identifying each item is placed; and the additional information storage section a search item designation area in which an item to be next subjected to associative search is stored in accordance with a target line (col. 10, lines 24-60 and col. 8, lines 1-59).

Response to Arguments

36. Applicant's arguments filed 5/18/2010 and 6/18/2010 have been fully considered but they are not persuasive.

37. Applicant's Argument:

"In this regard, Applicant respectfully contends that this amendment to claim 1 now clearly distinguishes over Miki. and/or Miki in view of Huang for at least the following reasons: First of all, the memory disclosed and discussed by Miki is not a "dependency relations information storage" of the type recited in Applicant's claims as defined by Applicant's specification. In contrast to Miki's memory, Applicant's dependency relations information storage stores "dependency relations" information regarding I/O data patterns for groups of instructions as opposed to Miki's storage of only past execution results, *Second, Miki does not teach or disclose any particular details of how specific input and output elements are derived or disclose or suggest a means to identify the particular input elements from which each output element is derived.* This deficiency is not rectified by the Huang '909 reference because Huang, at best, describes only the very general relationship between input elements and the output elements, and only for the instance of execution of one or more specific program instructions in the instruction region. Consequently, neither Miki nor Huang teach or suggest Applicant's "dependency relations information" limitation as currently set forth in Applicant's claim 1 for indicating the value and address of the particular input element in the input pattern from which each output element is derived."

Examiner's Response:

The examiner respectfully disagrees because the applicant did not explicitly define the 'dependency relations information storage'. However, it's understood to be a storage that stores dependency information which was explicitly shown in Mike, col. 2, lines 8-44. Mike's memory stores data that results from instruction dependency which reads on applicant's dependency relations information storage. However, Mike did not describe the detail of input/output elements. However, the secondary reference Huang teaches indication which input element in the input pattern each output element in the output pattern derives; and input/output group setting means for setting, based on stored dependency relations information, an input/output group that is made up of an

output pattern including at least one said output element and an input pattern including at least one said input element (see Huang, Fig. 3 and col. 5, lines 16-51).

Furthermore, Miki shows a memory that stores result of instruction dependency but Miki's did not show the detail on the input/output elements pattern. However, Huang shows input/element pattern with respect to the dependency relation information, thus combining both reference reads on applicant's claim language. Furthermore, the examiner would like to remind the applicant's that a rejection is based on the broadest reasonable interpretation of the claim language along with explicit and unambiguous definitions for the claim language which must be made available in the specification. The instant application did not provide any explicit definitions for the argued elements of claim 1, including the dependency relation information storage.

Conclusion

38. Any inquiry concerning this communication or earlier communications from the examiner should be directed to IDRISS N. ALROBAYE whose telephone number is (571)270-1023. The examiner can normally be reached on Mon-Fri from 8:00 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Idriss N Alrobaye/
Examiner, Art Unit 2183